AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

Claims 1-22 (canceled).

23. (withdrawn): A manufacturing method of a semiconductor memory device having a memory cell array portion and a peripheral transistor portion, said memory cell array portion having a source area formed by a self-aligned process, comprising:

forming an isolation insulating film on a semiconductor substrate, said isolation insulating film having a plurality of openings, each of said openings having a rectangular shape being elongate in a first direction, said openings being arranged in a second direction crossing said first direction;

forming tunnel insulating films on said semiconductor substrate in said openings;

forming a plurality of word lines on said isolation insulating film and said tunnel insulating films, each of said word lines being elongate in said second direction, said word lines being arranged in said first direction, and forming a plurality of floating gates sandwiched between said word lines and said tunnel insulating films, said floating gates being arranged at intersections of said openings and said word lines, wherein said plurality of word lines comprise at least a first word line and a second word line arranged on the same tunnel insulating films, and wherein said plurality of word lines provide said source area sandwiched between said first word line and said second word line, and a drain area disposed on the other side of said first word line

than a side of said source area and disposed on the other side of said second word line than a side of said source area;

removing said isolation insulating film and said tunnel insulating film at said source area to expose said semiconductor substrate having an uneven surface, while said isolation insulating film and said tunnel insulating films are kept on said semiconductor substrate at said drain area;

forming a mask on said source area having said uneven surface;

covering said semiconductor substrate at least at said peripheral transistor portion with a metal film and performing a heat treatment to form a silicide film on said peripheral transistor portion.

24. (withdrawn): The method as claimed in claim 23, wherein said mask is formed in a thickness so that a space between said mask on a side surface of said first word line and said mask on a side surface of said second word line facing said side surface of said first word line is left while a surface of said source area is covered with said mask.

25. (withdrawn): The method as claimed in claim 24, wherein said mask covers said surface of said source area and top surfaces of said first and second word lines, during the step of covering said semiconductor substrate with said metal film.

26. (withdrawn): The method as claimed in claim 24, wherein said mask covers said surface of said source area and

wherein said top surfaces of said first and second word lines are free from said mask, during the step of covering said semiconductor substrate with said metal film.

27. (withdrawn): The method as claimed in claim 23, wherein said mask is formed such that a space between a side surface of said first word line and a side surface of said second word line facing with said side surface of said first word line is filled with said mask.

28. (withdrawn): The method as claimed in claim 27, wherein said mask covers said surface of said source area and top surfaces of said first and second word lines, during the step of covering said semiconductor substrate with said metal film.

29. (withdrawn): The method as claimed in claim 28, wherein said mask consists of one layer.

30. (withdrawn): The method as claimed in claim 29, wherein a step of forming said mask comprises:

forming a first mask so that said space is left; and then

forming a second mask so that said space is filled with said second mask, wherein said mask comprises said first mask and said second mask.

Claim 31 (canceled).

32. (currently amended): A method of manufacturing a semiconductor device, comprising:

selectively forming in a semiconductor substrate first, second, third, fourth, fifth and sixth diffusion regions apart from one another, said first and second diffusion regions constituting a first memory cell having a first floating gate over a first channel region sandwiched between said first and second diffusion regions and a first control gate over said first floating gate, said second and third diffusion regions constituting a second memory cell having a second floating gate over a second channel region sandwiched between said second and third diffusion regions and a second control gate over said second floating gate, said fourth and fifth diffusion regions constituting a third memory cell having a third floating gate over a third channel region sandwiched between said fourth and fifth diffusion regions and a third control gate over said third floating gate, said fifth and sixth diffusion regions constituting a fourth memory cell having a fourth floating gate over a fourth channel region sandwiched between said fifth and sixth diffusion regions and a fourth control gate over said fourth floating gate;

forming a mask layer to cover a surface of said second ~~and fifth diffusion regions~~ region with leaving top surfaces of said first, second, third and fourth control gates and surfaces of said first, third, fourth and sixth diffusion regions uncovered;

forming a silicide layer on said top surface of said first, second, third and fourth control gates and said surfaces of said first, third, ~~fourth~~ fifth and sixth diffusion regions, said surfaces of

said second ~~and fifth diffusion regions~~ region being free from formation of said silicide region by existence of said mask layer.

Claims 33-37 (canceled).

38. (previously presented): The method as claimed in claim 32, further comprising:

forming an interlayer film over said semiconductor substrate after forming said silicide layer;

forming a source line wiring on said interlayer film and a source contact connecting said source line wiring with said silicide layer on said fifth diffusion region.

39. (new): A method of manufacturing a semiconductor memory devise, comprising:

selectively forming in a semiconductor substrate first, second third, fourth, fifth and sixth diffusion region apart from one another, said first and second diffusion regions constituting a first memory cell having a first floating gate over a first channel region sandwiched between said first and second diffusion regions and a first control gate over said first floating gate, said second and third. diffusion regions constituting a second memory cell having a second floating gate over a second channel region sandwiched between said second and third diffusion regions and a second control gate over said second floating gate, said fourth and fifth diffusion regions constituting a third memory cell having a third floating gate over a third channel region

sandwiched between said fourth and fifth diffusion regions and third control gate over said third floating gate, said fifth and sixth diffusion regions constituting a fourth memory cell having a fourth floating gate over a fourth channel region sandwiched between said fifth and sixth diffusion regions and a fourth control gate over said fourth floating gate;

forming an insulating layer to cover a surface of said first, second, third diffusion layers., a surface of said first and second control gates, a sidewall of said third floating gate and third control gate and a sidewall of said fourth floating gate and fourth control gate with leaving top surface of said third and fourth control gates and a surface of said fourth, fifth and sixth diffusion layers uncovered; and

forming a silicide layer on said top surface of said third and fourth control gates and a surface of said fourth, fifth and sixth diffusion layers, said surface of said first, second and third diffusion layers being free from formation said silicide region by existence of said insulating layer.

40. (new): A method of manufacturing a semiconductor memory devise, comprising:

selectively forming in a semiconductor substrate first, second third, fourth, fifth and sixth diffusion region apart from one another, said first and second diffusion regions constituting a first memory cell having a first floating gate over a first channel region sandwiched between said first and second diffusion regions and.a first control gate over said first floating gate, said second and third diffusion regions constituting a second memory cell having a second floating gate over a second channel region sandwiched between said second and third diffusion regions and a

second control gate over said second floating gate, said fourth and fifth diffusion regions constituting a third memory cell having a third floating gate over a third channel region sandwiched between said fourth and fifth diffusion regions and third control gate over said third floating gate, said fifth and sixth diffusion regions constituting a fourth memory cell having a fourth floating gate over a fourth channel region sandwiched between said fifth and sixth diffusion regions and a fourth control gate over said fourth floating gate;

forming a sidewall to cover a sidewall of said first floating gate and said first control gate, a sidewall of said second floating gate and said second control gate, a sidewall of said third floating gate and third control gate and a sidewall of said fourth floating gate and fourth control gate with leaving top surface of said first, second, third and fourth control gates and a surface of said first, second, third, fourth, fifth and sixth diffusion layers uncovered;

forming an insulating layer to fill up a space sandwiched between said sidewall of said first floating gate and said first control gate and said sidewall of said second floating gate and said second control gate with leaving top surface of said first, second, third and fourth control gates said surface of said first, third, fourth, fifth and sixth diffusion regions uncovered; and

forming a silicide layer on said top surface of said first, second, third and fourth control gates and a surface of said first, third, fourth, fifth and sixth diffusion layers, said surface of said second diffusion layer being free from formation said silicide region by existence of said insulating layer.

41. (new): The method as claimed in claim 32, said first, second and third diffusion regions being formed in a memory cell portion, and said fourth, fifth and sixth diffusion regions being formed in source contact portion.

42. (new): The method as claimed in claim 39, said first, second and third diffusion regions being formed in a memory cell portion, and said fourth, fifth and sixth diffusion regions being formed in source contact portion.

43. (new): The method as claimed in claim 40, said first, second and third diffusion regions being formed in a memory cell portion, and said fourth, fifth and sixth diffusion regions being formed in source contact portion.